WHAT IS CLAIMED IS:

1. A test apparatus for testing an electronic device, comprising:

a reference clock generating unit for generating a reference clock;

a pattern generating unit for generating a test pattern synchronously with said reference clock to test said electronic device;

a waveform formatting unit for receiving said test pattern and inputting a formatted pattern which results from formatting said test pattern to said electronic device;

a first timing generator for generating a timing signal;

an output signal sampling circuit for sampling an output signal outputted by said electronic device in response to said test pattern at timing based on said timing signal generated by said first timing generator; and

a judging unit for judging quality of said electronic device based on a sampling result of said output signal sampling circuit,

wherein said first timing generator comprises:

a first variable delay circuit unit for receiving, delaying and outputting said reference clock; and

a first delay control unit for controlling a delay amount of said first variable delay circuit unit, and

said first delay control unit comprises:

a first basic timing data setting unit to which a first basic timing data is set in advance;

a first multi-strobe resolution data setting unit to which a first multi-strobe resolution data is set in advance;

a first multi-strobe data calculating unit for calculating a first multi-strobe data based on said first multi-strobe resolution data in response to said reference clock; and

a first variable delay amount calculating unit for calculating said delay amount, by which said reference clock is to be delayed in said first variable delay circuit unit, based on said first basic timing data and first multi-strobe data.

2. A test apparatus as claimed in claim 1, wherein said judging unit comprises output signal jitter calculating means for calculating jitter of said output signal based on said sampling result of said output signal sampling circuit, and judges quality of said electronic device further based on said jitter of said output signal.

3. A test apparatus as claimed in claim 1, wherein said first variable delay amount calculating unit calculates said delay amount by adding said first multi-strobe data to said first basic timing data.

4. A test apparatus as claimed in claim 1, wherein said first variable delay amount calculating unit calculates said delay amount by subtracting said first multi-strobe data from said first basic timing data.

5. A test apparatus as claimed in claim 1, wherein said first delay control unit further comprises:

a first multi-strobe data storing unit for storing said first multi-strobe data calculated by said first multi-strobe data calculating unit; and

a first multi-strobe resolution data adding unit for adding said first multi-strobe resolution data to said first multi-strobe data stored in said first multi-strobe data storing unit in response to said reference clock,

said first multi-strobe data storing unit stores anew said first multi-strobe data to which said first multi-strobe resolution data has been added by said first multi-strobe resolution data adding unit, and

said first variable delay amount calculating unit calculates said delay amount, by which said reference clock is to be delayed in said first variable delay circuit unit, based on said first basic timing data and said first multi-strobe data stored in said first multi-strobe data storing unit.

6. A test apparatus as claimed in claim 1, wherein said pattern generating unit further comprises means for setting said first multi-strobe data stored in said first multi-strobe data storing unit to be zero based on said test pattern generated by said pattern generating unit.

7. A test apparatus as claimed in claim 1, further comprising means for setting a new first basic timing data in said first basic timing data setting unit, when a test cycle to test said electronic device is completed.

8. A test apparatus as claimed in claim 1, wherein said pattern generating unit further comprises means for setting

a new first multi-strobe resolution data in said first multi-strobe resolution data setting unit based on said test pattern generated by said pattern generating unit.

9. A test apparatus as claimed in claim 1, further comprising:

a second timing generator for generating a timing signal; and

a data strobe sampling circuit for sampling a data strobe at timing based on said timing signal generated by said second timing generator,

wherein said electronic device outputs said output signal and said data strobe which is for an external apparatus to receive said output signal in response to an internal clock,

said second timing generator comprises:

a second variable delay circuit unit for receiving, delaying and outputting said reference clock; and

a second delay control unit for controlling a delay amount of said second variable delay circuit unit,

said second delay control unit comprises:

a second basic timing data setting unit to which a second basic timing data is set in advance;

a second multi-strobe resolution data setting unit to which a second multi-strobe resolution data is set in advance;

a second multi-strobe data calculating unit for calculating a second multi-strobe data based on said second multi-strobe resolution data in response to said reference clock; and

a second variable delay amount calculating unit for calculating said delay amount, by which said reference

clock is to be delayed in said second variable delay circuit unit, based on said second basic timing data and second multi-strobe data, and

said judging unit judges quality of said electronic device further based on a sampling result of said data strobe sampling circuit.